

METHOD FOR FABRICATING A VERTICAL BIPOLAR JUNCTION TRANSISTOR

Abstract

A semiconductor wafer includes a first doping region of a first conductivity type, a second doping region of a second conductivity type, and a plurality of isolated structures positioned on surfaces of the first doping region and the second doping region. A third doping region of the first conductivity type is formed in an upper portion of the second doping region. A shielding layer is formed and a portion of the shielding layer is removed to form an opening shielding layer to expose a portion of the third doping region. Subsequently, a doping layer of the second conductivity type is formed on a surface of the third doping region. A self-aligned silicidation process is performed to form a silicide layer on the surfaces of the second doping region, the third doping region and the doping layer, the silicide layer functioning as a contact region of a vertical bipolar junction transistor.